decreased by the voltage drop across resistor R15, and increased by the voltage drop across resistor R14, respectively. The voltage drops across resistors R14 and R15 depend upon the current mirrored there through by transistors Q12 and Q15. Thus the voltage at the positive input to comparators **80** and **82** is adjustable by the external resistor R16 coupled to the terminal TSET.

The negative input to comparators **80** and **82** is provided by the output of amplifier **68**, which as previously described, provides an output proportional to the rate of change of the output voltage Vout, more specifically, an increasing output voltage for increasing rates in the drop of the output voltage Vout and a decreasing output voltage for increases in the rate of increase of the output voltage Vout. Assume for the moment that a large load is suddenly imposed on the converter, causing the output voltage Vout to begin to rapidly drop. This will drive the output of amplifier **68** sufficiently high to force the output of comparator **82**, which is normally high, to go low. This forces the output of NAND gate **54** high, turning off n-channel power device N1 if it was on, and turning on p-channel power device P1, independent of the state of the respective pulse width modulator. Similarly, n-channel power device N2 will be turned off if it was on, and p-channel power device P1 will be turned on, independent of the state of that pulse width modulator. Of course, once the rate of drop of the output voltage Vout reduces, the output of comparator **82** will again go high, allowing the interleaved pulse width modulators to resume control of the output devices.

Similarly, if a large load is suddenly removed so that the output voltage Vout starts to rapidly increase, the output of amplifier **68** will drop sufficiently so that the output of comparator **80** will go high. This forces the output of NOR gate **46** to go low, the output of NAND gate **50** to go high, and the output of NAND gate **54** to go low (the other input thereto normally being high), turning off p-channel power device P1 if the same was on, and then turning on n-channel power device N1. In a similar manner, the high output of comparator **80** will simultaneously turn off p-channel power device P2 if the same was on, and turn on n-channel power device N2. Thus, in normal operation the converters operate in an interleaved fashion to provide, in an integrated form, all the herein before stated advantages of interleaved converters. However, in the event of extraordinary rates of change in the converter output voltage Vout, the converters switch to act in unison to respond to the extraordinary conditions, independent of the state of the interleaved pulse width modulators, to minimize the converter output voltage swing with extraordinary changes in load.

Also shown in FIG. **2** is a circuit for monitoring the error between the output of the MDAC and Vout, and for controllably reading the MDAC output. More specifically, the output of the MDAC and Vout are applied as the two inputs to window comparator **120**, which provides a high output Voutok whenever the output voltage is within acceptable limits. This signal is applied as one input to NAND gate **122**. The second input to NAND gate **122** is the input signal output-enable/$\overline{\text{shutdown}}$ OUTEN/SHDNB. When the output enable signal is low, the output of inverter **124** will be high, providing the shut down signal SHDN to shut down the rest of the circuit (the details of shut down circuitry in general are well known in the prior art and not part of the invention claimed herein). When the output enable signal is high, both inputs to NAND gate **122** will be high if the error signal is within acceptable limits, making the output of NAND gate **122** low, holding the output of AND gate **126** low and holding transistor Q16 off. Under these conditions, inverter

130 provides a high signal to the startup and overload circuit **22**, indicating that the error signal is within acceptable limits. If the error signal moves out of acceptable limits, the signal Voutok will go low, driving the output of NAND gate **122** high. Since the high state of the output enable signal is substantially equal to the analog voltage V, transistor Q7 will be off so that the resistor **R16** will pull the input to inverter **134** low. This forces the second input to AND gate **126** high also, turning on transistor **Q16** to indicate to the system connected thereto that the error signal between the commanded output voltage and the then existing output voltage is excessive.

For test purposes, the output enable signal may be driven above the analog voltage V so as to turn on transistor Q7. This pulls the input to inverter **134** high, driving the output of the inverter low, in turn making the output of AND gate **126** low and holding transistor Q16 off. The high voltage on the input to inverter **134** also controls a multiplexer **136** to couple the output of the MDAC to the output pin PWRGD. Thus, the output pin PWRGD can be used for test purposes, to monitor the output of the MDAC to verify that the MDAC and the control thereto is working as intended. Driving the output enable signal above the analog voltage V, of course, does not otherwise affect the operation of the circuit, so that normal circuit operation will continue without interruption.

The preferred embodiment of the present invention has been disclosed with respect to interleaved buck converters for purposes of specificity in the illustrative embodiment. The principles of the invention are not limited to such inverters, however, and may also readily be adapted to boost or step up converters by one of ordinary skill in the art. Similarly, while a dual interleaved inverter has been disclosed, the principles of the invention may be applied to interleaved converters having more than two converters being interleaved. Thus while a certain exemplary embodiment has been described in detail and shown in the accompanying drawings, it is to be understood that such embodiment is merely illustrative of and not restrictive on the broad invention, and that this invention is not to be limited to the specific arrangements and constructions shown and described, since various other modifications may occur to those with ordinary skill in the art.

What is claimed is:

1. A DC to DC switching circuit for controlling power switching devices in a DC to DC converter having first and second interleaved converter circuits operating into a common load comprising:

- a current sense circuit sensing the voltage across a sense resistor in series with the power supply supplying power to the power switching devices;
- a first pulse width modulator controlling the power switching devices of the first converter circuit;
- a second pulse width modulator controlling the power switching devices of the second converter circuit;
- a feedback circuit responsive to the voltage across the common load;
- control circuits for controlling the first and second pulse width modulators responsive to the feedback circuit and a commanded output voltage;
- the control circuits also being responsive to the difference in the voltage across the sense resistor when the first converter is drawing power from the power supply through the sense resistor and the second converter is not, and when the second converter is drawing power from the power supply through the sense resistor and the first converter is not, to adjust the relative duty

cycle of the first and second converters to tend to minimize the difference in the voltage across the sense resistor;

the current sense circuit, the first pulse width modulator, the second pulse width modulator, the feedback circuit and the control circuits being in a single integrated circuit.

2. The DC to DC switching circuit of claim **1** wherein the sense resistor is external to the integrated circuit.

3. The DC to DC switching circuit of claim **1** further comprised of an integrator having an output responsive to the integral of an error signal, the error signal being responsive to the voltage across the common load and a desired voltage, the control circuits also being responsive to the output of integrator.

4. The DC to DC switching circuit of claim **3** wherein the time constant of the integrator is adjustable by the selection of at least one component external to the integrated circuit.

5. The DC to DC switching circuit of claim **3** further comprised of a differentiator having an output responsive to the rate of change of the voltage across the common load, the control circuits also being responsive to the output of differentiator.

6. The DC to DC switching circuit of claim **5** wherein the time constant of the differentiator is adjustable by the selection of at least one component external to the integrated circuit.

7. The DC to DC switching circuit of claim **1** wherein the control circuits are also responsive to rapid decreases in the voltage on the common load to turn on the first and second converter circuits independent of the phase of the first and second pulse width modulators.

8. The DC to DC switching circuit of claim **7** wherein the control circuits are also responsive to rapid increases in the voltage on the common load to turn off the first and second converter circuits independent of the phase of the first and second pulse width modulators.

9. The DC to DC switching circuit of claim **1** further comprised of a load variation circuit coupled to the control circuits to decrease the voltage on the common load for higher voltages across the current sense resistor and to increase the voltage on the common load for lower voltages across the current sense resistor.

10. DC to DC switching circuit for controlling power switching devices in a DC to DC converter having first and second interleaved converter circuits operating into a common load comprising:

a first pulse width modulator controlling the power switching devices of the first converter circuit;

a second pulse width modulator controlling the power switching devices of the second converter circuit;

a feedback circuit responsive to the voltage across the common load;

control circuits for controlling the first and second pulse width modulators responsive to the feedback circuit;

the control circuits also being responsive to the difference in current through the first converter and the second converter to adjust the relative duty cycle of the first and second converters to tend to minimize the difference in the voltage across the sense resistor;

the current sense circuit, the first pulse width modulator, the second pulse width modulator, the feedback circuit and the control circuits being in a single integrated circuit.

11. The DC to DC switching circuit of claim **10** wherein the commanded output voltage is controllable through an input to the integrated circuit.

12. The DC to DC switching circuit of claim **10** wherein the commanded output voltage is controllable through a digital input to the integrated circuit.

13. The DC to DC switching circuit of claim **12** further comprised of an integrator having an output responsive to the integral of an error signal, the error signal being responsive to the voltage across the common load and a desired voltage, the control circuits also being responsive to the output of integrator.

14. The DC to DC switching circuit of claim **13** wherein the time constant of the integrator is adjustable by the selection of at least one component external to the integrated circuit.

15. The DC to DC switching circuit of claim **13** further comprised of a differentiator having an output responsive to the rate of change of the voltage across the common load, the control circuits also being responsive to the output of differentiator.

16. The DC to DC switching circuit of claim **15** wherein the time constant of the differentiator is adjustable by the selection of at least one component external to the integrated circuit.

17. The DC to DC switching circuit of claim **12** wherein the control circuits are also responsive to rapid decreases in the voltage on the common load to turn on the first and second converter circuits independent of the phase of the first and second pulse width modulators.

18. The DC to DC switching circuit of claim **17** wherein the control circuits are also responsive to rapid increases in the voltage on the common load to turn off the first and second converter circuits independent of the phase of the first and second pulse width modulators.

19. The DC to DC switching circuit of claim **12** further comprised of a load variation circuit coupled to the control circuits to decrease the voltage on the common load for higher currents through the converters and to increase the voltage on the common load for lower currents through the converters.

20. The DC to DC switching circuit of claim **12** wherein the commanded output voltage is controllable through an input to the integrated circuit.

21. The DC to DC switching circuit of claim **12** wherein the commanded output voltage is controllable through a digital input to the integrated circuit.

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